

**Chapter 1 : Number Systems and Logic Gates****1-1 to 1-50****Syllabus :** Review of number systems, Logic gates.

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### Chapter 3 : Combinational Logic Circuit Design

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**Chapter 7 : Introduction to Finite State Machines****7-1 to 7-18**

**Syllabus :** Introduction to Finite State Machines (FSM) :  
The need for state machines, The state machine, Basic  
concepts in state machine analysis.

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**Chapter 8 : Synchronous State Machine Design****8-1 to 8-50**

**Syllabus :** Sequential counters, State changes referenced  
to clock, Number of state flip-flops, Input forming logic,  
Output forming logic, Generation of a state diagram from a  
timing chart, Redundant states, General state machine  
architecture, Concept of asynchronous state machine and  
comparison to synchronous state machine.

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#### **Chapter 11 : Introduction to Verilog HDL    11-1 to 11-24**

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