Chapter 1 : Number Systems and Logic Gates

1-1 to 1-50

Syllabus : Review of number systems, Logic gates.

Syllabus : Boolean algebra : Postulates and theorems, SOP and POS forms, Canonical forms, Logic minimization using Karnaugh map and tabulation methods upto 6 variables, Realizing logic functions using gates.

Chapter 3 : Combinational Logic Circuit Design 3-1 to 3-63

Syllabus : Half adder, Full adder, BCD adder, Code converters, Magnitude comparator, Multiplexers and decoders, MSI digital circuit design problems.

Syllabus : Sequential logic circuit design : Flip-flops-SR, JK, T, D and Master slave Flip flops.

Chapter 7 : Introduction to Finite State Machines **7-1 to 7-18**

Syllabus : Introduction to Finite State Machines (FSM) : The need for state machines, The state machine, Basic concepts in state machine analysis.

Chapter 8 : Synchronous State Machine Design **8-1 to 8-50**

Syllabus : Sequential counters, State changes referenced to clock, Number of state flip-flops, Input forming logic, Output forming logic, Generation of a state diagram from a timing chart, Redundant states, General state machine architecture, Concept of asynchronous state machine and comparison to synchronous state machine.

Chapter 9 : Logic Families 9-1 to 9-30

Syllabus : Specifications, Noise margin, Propagation delay, Fan-in, Fan-out, Transistor-Transistor Logic (TTL), Emitter Coupled Logic (ECL), CMOS logic, TTL and CMOS gates, Introduction to basics of FINFET.

Chapter 10 : Programmable Logic Devices 10-1 to 10-30

Syllabus : Introduction to Programmable Logic Devices, Read-Only Memory, Programmable Logic Arrays (PLA), Programmable Array Logic (PAL), Combinational PLD Based State Machines, State Machines on a Chip.

Syllabus : VLSI design flow : Design entry : Schematic, FSM and HDL, Different modeling styles in verilog : Behavioral and structural modeling, Data types and objects, Synthesis and simulation verilog constructs and codes for combinational and sequential circuits.

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