Chapter 1 : Number Systems and Logic Gates

1-1 to 1-50

Syllabus : Review of number systems, Logic gates.

Syllabus : Boolean algebra : Postulates and theorems, SOP and POS forms, Canonical forms, Logic minimization using Karnaugh map and tabulation methods upto 6 variables, Realizing logic functions using gates.

Chapter 11 : Introduction to Verilog HDL 11-1 to 11-24

Syllabus : VLSI design flow : Design entry : Schematic, FSM and HDL, Different modeling styles in verilog : Behavioral and structural modeling, Data types and objects, Synthesis and simulation verilog constructs and codes for combinational and sequential circuits.

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